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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/767,231	01/22/2001	Takehiko Nomura	IGARA9.001AUS	1471

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EXAMINER
KIANNI, KAVEH C

ART UNIT	PAPER NUMBER
2877	

DATE MAILED: 05/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/767,231	NOMURA ET AL.	
	Examiner	Art Unit	
	Kevin C Kianni	2877	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to because certain/essential elements of the drawings in figures 1-7 are not labeled. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arai et al. (US 5150280).

Regarding claim 1, Arai teaches a silicon platform for optical modules (shown in figures 1, items 20 and 16) comprising: a silicon substrate (fig. 18, item 16); a first insulating layer formed on the silicon substrate (fig. 18, item120; col. 14, lines 42-54; wherein the first insulation layer is formed on the substrate of the chip in which the substrate is silicon, see col. 2, lines 59-60, also col. 20, lines 8-10); a first conductor layer formed on the first insulating layer (col. 14, lines 42-54; wherein alternately, the first conductor layer is formed on the first insulation layer); a second insulating layer formed on the first conductor layer (col. 14, lines 42-54; wherein alternately, the second

insulation layer is formed on the first conductor layer); and a conductor layer formed on the second insulating layer (col. 14, lines 42-54; wherein alternately, the second conductor layer is formed on the second insulation layer). Arai further teaches conductor layer overlying the first insulating layer (see fig. 18, items insulator 50 and the conductor/ground 58; col. 8, lines 14-15 and col. 14, lines 20-21) to constitute bonding portions connected to lead wires (fig. 18, item 118). However, Arai does not explicitly state that the above underlined limitation is the end portion of the second conductor layer. It is obvious to a person of ordinary skill in the art that first conducting/ground layer overlying (note that overlying is not synonym as attached) the chip/silicon substrate is an end portion of the second or third conducting layer 58/62 through the extended ground strips 64 that connects these conducting/ground layers together provided that the chip/silicon substrate layer is the first insulation layer (see col. 14, lines 17-26 and col. 15, lines 24-33), since this configuration of layers over the chip/silicon substrate restrain a high speed characteristic deterioration and controls heat radiation (see col. 2, lines 66-68).

Regarding claim 2, Arai further teaches wherein a hole is formed in the second insulating layer and a bonding portion is formed in this hole (see fig. 18, wherein the bonding is formed in a hole surrounded by the insulation layer 50, provided that the silicon substrate acts as the first insulation layer).

Regarding claim 3, Arai further teaches wherein a removed portion is formed in the second insulating layer and a bonding portion is formed in this removed portion (see fig. 18, wherein the bonding is formed in a hole surrounded by the insulation layer 50).

Regarding claim 4, Arai teaches all limitations of claim 1. However, Arai does not specifically state that wherein the second insulating layer has a thickness of 6 μm or less. Nevertheless, Arai states that thickness of the layers, including the second layer is optimized according to the thickness/length of the chip. Thus, it has been obvious to a person of ordinary skill in the art to modify the thickness of the second insulation layer of Arai to a conventional thickness of 6 μm or less since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 5, Arai further teaches wherein optical elements are mounted and an end portion of the second conductor layer lies right below the optical elements (see fig. 11-12, items 76, 98 and 76; col. 13, lines 13-21).

Regarding claim 6, Arai further teaches wherein a bulky portion is formed on part of the first insulating layer (fig. 11, items 98 and 30).

Regarding claim 7, Arai further teaches wherein the first conductor layer, the second insulating layer and the second conductor layer constitute a microstrip line

structure (shown in fig. 18, items 120 also items 52, 62 and 58 constitute microstrip line structure consisting of layers of conducting and insulation layers).

Regarding claim 8, Arai teaches all limitations of claim 1. Arai further teaches a silicon-based chip that the second conducting layer 58 includes includs distribution constant circuit structure, as shown in fig. 18. However, Arai does not teach wherein the above underlined layer is a coplanar structure. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the structure of Arai's second conducting layer structure so as it resembles a coplanar structure. since it has been held that the provision of adjustability, where needed, involves only routine skill in the art. In re Stevens, 101 USPQ 284 (CCPA 1954).

Regarding claim 9, Arai further teaches silicon platform for optical modules according to claim 1, which is electrically connected to a driver IC by lead wires (see fig. 10, items 88 and 98; also col. 11, lines 18-21).

Regarding claim 10, Arai further teaches wherein at least one of a light emitting element and a light receiving element are mounted (see fig. 1 and 2, items 22 and 2; also col. 7, lines 15-30; wherein photodiode 2 receives light from the light emitting fiber).

4. Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arai et a. as applied to claims 1-10 above, and further in view of Tomonari et al. (US 6,384,509).

Regarding claims 11-14, Arai teaches all limitations that the base claim in which the claims depend on. However, Arai does not explicitly state that the material used for the first or second insulation layer is one of an oxide layer such as SiO2 or a resin layer or a polyimide layer. This limitation is taught by Tomonari. Tomonari teaches a silicon-based substrate that it includes the above underlined limitation (see col. 17, lines 30-38). Thus, Tomonari's method of insulation layer can suppress/protect applied stress on the silicon-based device layers (col. 6, lines 23-29). Thus, it has been obvious to a person of ordinary skill in the art when the invention was made to modify Arai's insulation layers by applying the insulation layer types taught by Tomonari in order to produce a silicon-based device/chip that includes the above underlined limitation, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Citation of Relevant Prior Art

5. Prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In accordance with MPEP 707.05 the following references are pertinent in rejection of this application since they provide substantially the same information disclosure as this patent does. These references are:

Yamada et al. .teaches insulation and conducting layers in a silicon substrate

Burrows et al. .teaches insulation and conducting layers in a silicon substrate

Shakuda 5555115 .teaches insulation and conducting layers in a silicon substrate in a hole and substantially coplanar.

Sugahara et al. .teaches insulation and conducting layers in a silicon substrate

Hsu et al. 6333598 . .teaches insulation and conducting layers in a silicon substrate

Ito Soichi 59029454 .teaches at least claim 1 (except for optical parts limitation; provided in form 1449).

Yoshimura et al. 6343171 .teaches insulation and conducting layers in a silicon substrate

Diem Bernard et al. WO 87045565 .teaches insulation and conducting layers in a silicon substrate

These references are cited herein to show the relevance of the apparatus/methods taught within this reference as prior art.

Contact Information

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaveh Cyrus Kianni whose telephone number is (703) 308-1216. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 6:00 p.m. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank Font, can be reached at (703) 308-4881.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 308-7722, (for formal communications intended for entry)

or:

(703) 308-7721, (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand delivered responses should be brought to Crystal Plaza 4, 2021 South Clark Place, Arlington, VA., Fourth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0956.

Kevin Cyrus Kianni
Patent Examiner
Group Art Unit 2877

Frank Font
Supervisory Patent Examiner
Group Art Unit 2877

May 15, 2002